

# Introduction to researches on On-Chip Network

Semiconductor System Lab, KAIST

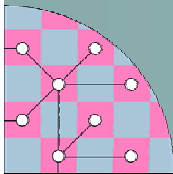
Hoi-Jun Yoo

2003. 10. 14

The logo for KAIST (Korea Advanced Institute of Science and Technology). It consists of the letters 'KAIST' in a bold, blue, sans-serif font. Below the letters, there is a blue horizontal oval shape.

# Outline

- Related works on networking
- Key technologies for OCN design
- project BONE
- Recent research topics



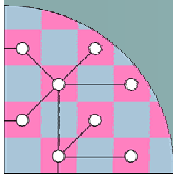
The background of the slide is a repeating pattern of a network diagram. Each diagram shows a central server rack connected to multiple client devices, with various network components like switches and routers. The diagrams are rendered in a light blue color on a darker blue background.

# **Related works on Networking**

# Switching System

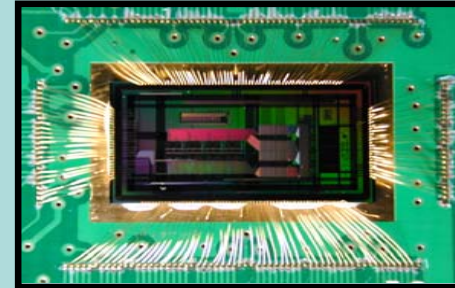
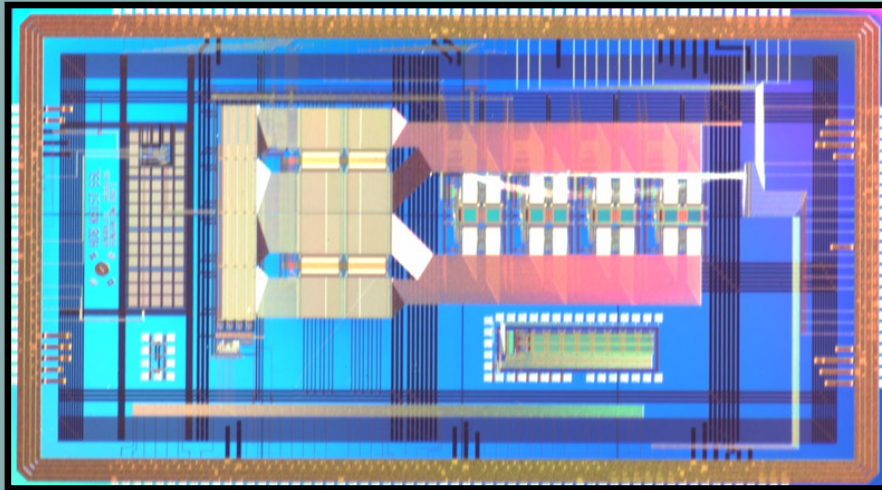
## ■ Theses & Conference papers

- ❑ Se-Joong Lee, “Performance Analysis of Gigabit Ethernet Shard-Memory Switch with Embedded DRAM,” M.S. Thesis, 2001
- ❑ Kangmin Lee, “Design and Implementation of an 80Gbps Shared Bus Packet Switching using Embedded DRAM,” M.S. Thesis, 2002
- ❑ Kangmin Lee, et al., “A practical method to use eDRAM in the shared bus packet switch,” GLOBECOM, 2002
- ❑ Kangmin Lee, et al., “A 10Gbps/port 8x8 Shared Bus Switch with embedded DRAM Hierarchical Output Buffer,” ESSCIRC 2003

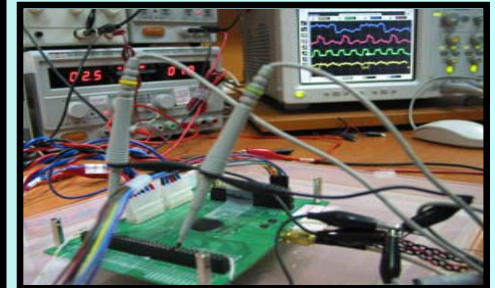


# Switching System (Cont'd)

## ■ 8x8 Shared-bus Switch Fabric for 10Gb-Ethernet



Chip on a Board



Measurement

Die Photo (4x9mm<sup>2</sup> @ 0.16um DRAM tech.)

- Hierarchical Output Buffering Technique (32kb SRAM & 1Mb DRAM)
- Dual I/O scheme

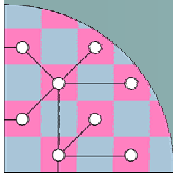
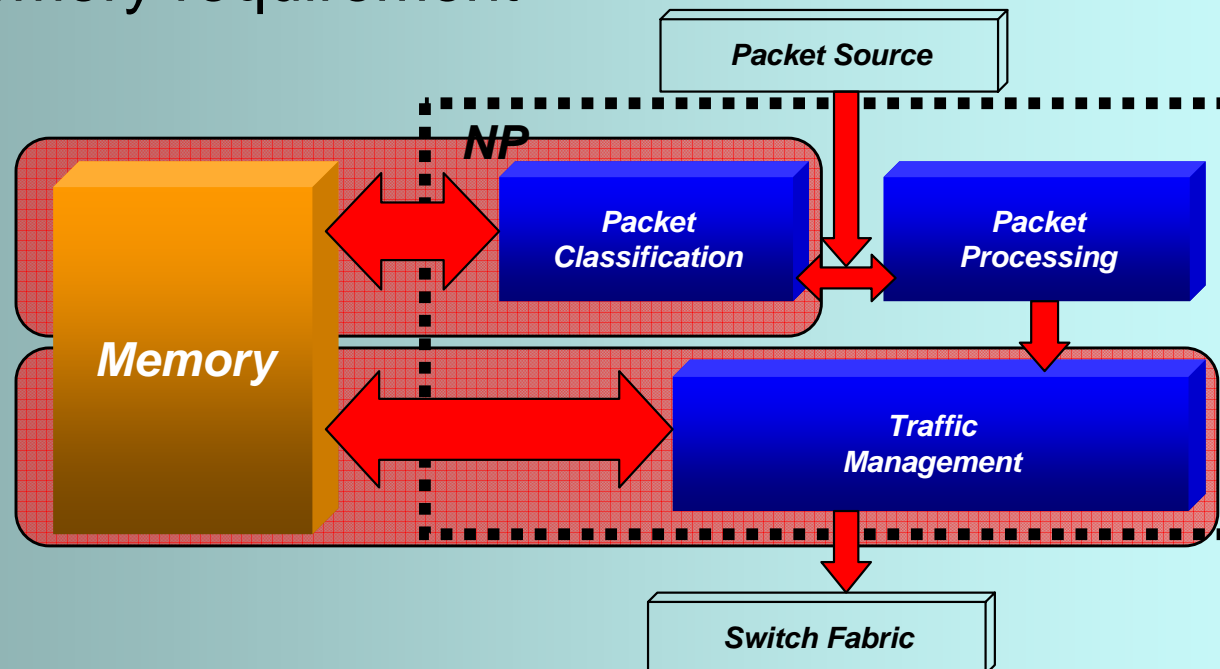
### Related papers

- [1] K. Lee, "A practical method to use eDRAM in the shared bus packet switch," GLOBECOM 2002
- [2] K. Lee, "A 10Gbps/port 8x8 Shared Bus Switch with embedded DRAM Hierarchical Output Buffer," ESSCIRC 2003

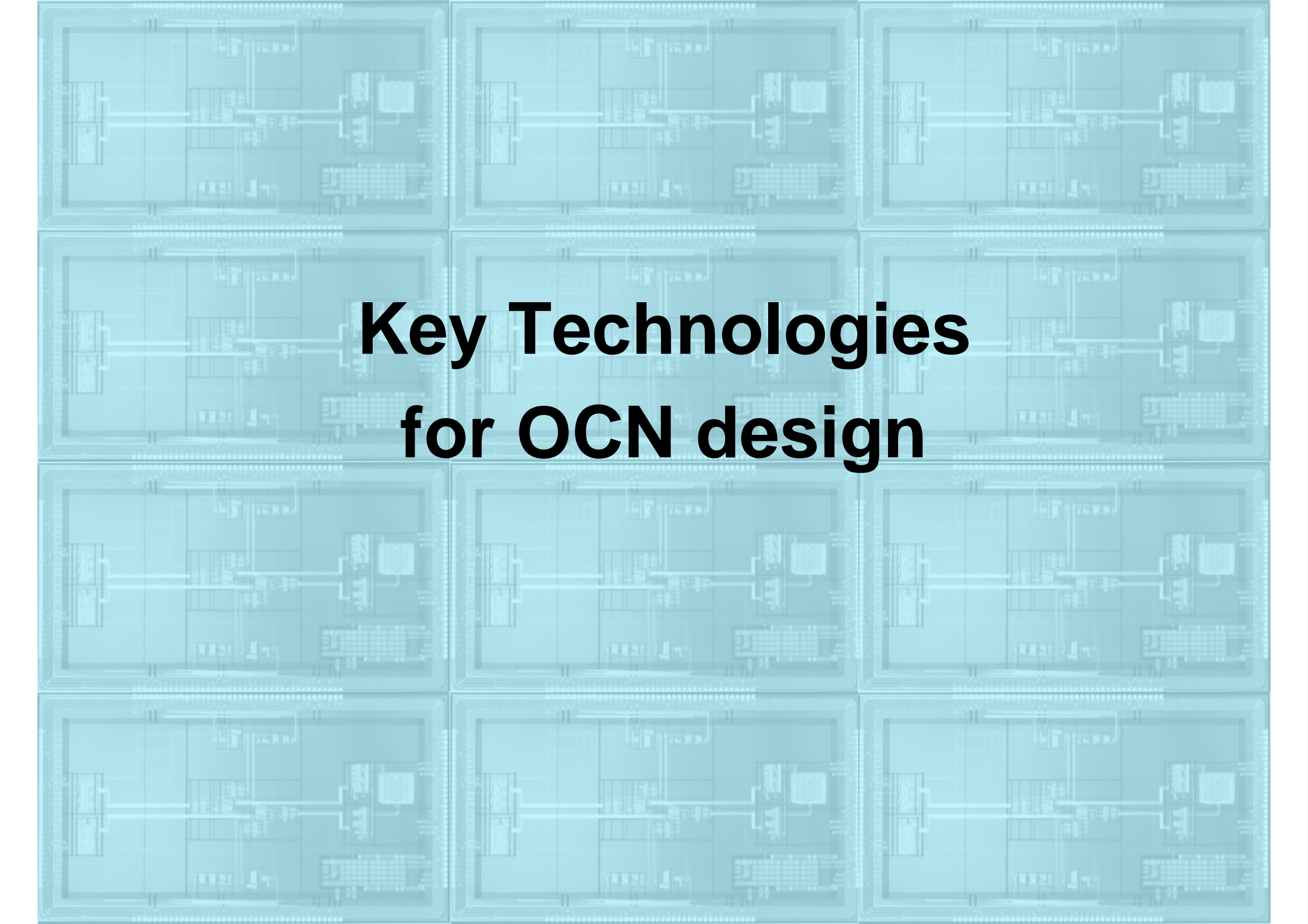
\* Best Design Award from 3<sup>rd</sup> Korea Semiconductor Layout Contest in 2002

# Network-related works (Cont'd)

- Network Processor
  - IP Address Lookup Engine
    - Algorithm
    - Implementation issues
    - Memory requirement

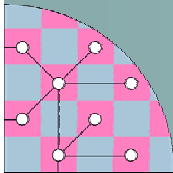
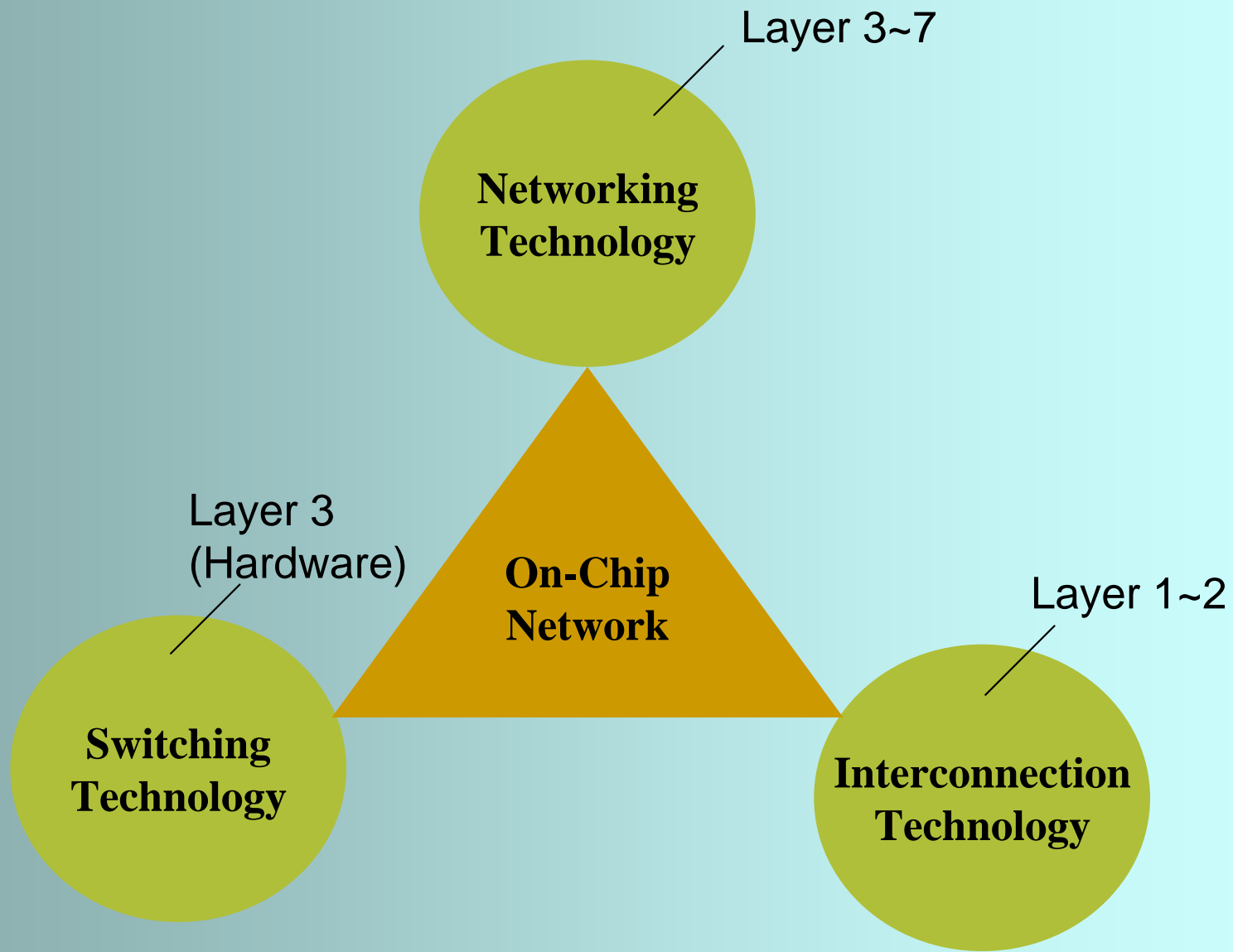




The background of the slide is a repeating pattern of circuit board layouts, specifically showing a grid of components and interconnecting lines in a light blue color. This pattern covers the entire slide area.

# **Key Technologies for OCN design**

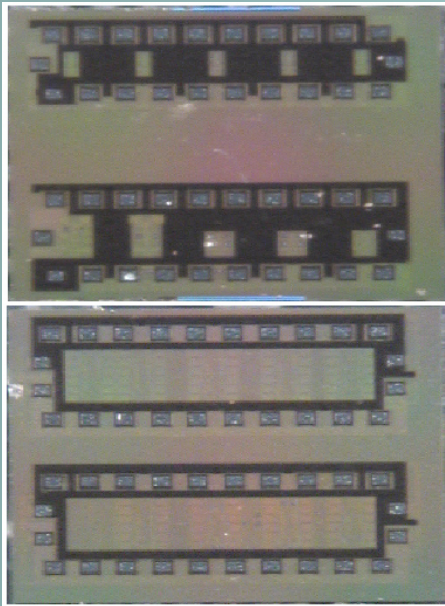
# Researches on OCN



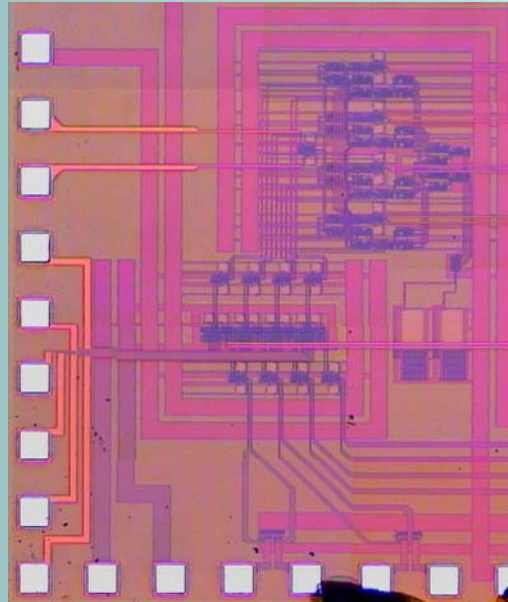


# Interconnection Technology

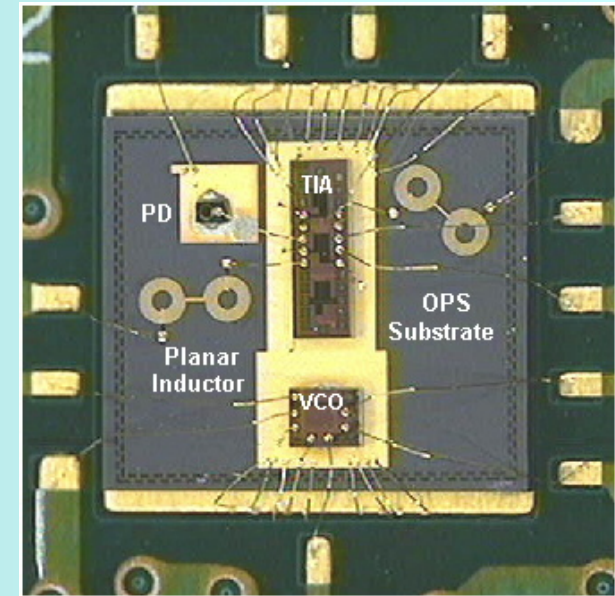
- High-speed serial link



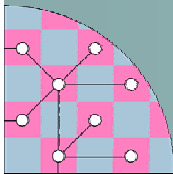
2.5Gb/s LVDS  
transmitter &  
1.3Gb/s receiver



4Gb/s CDR



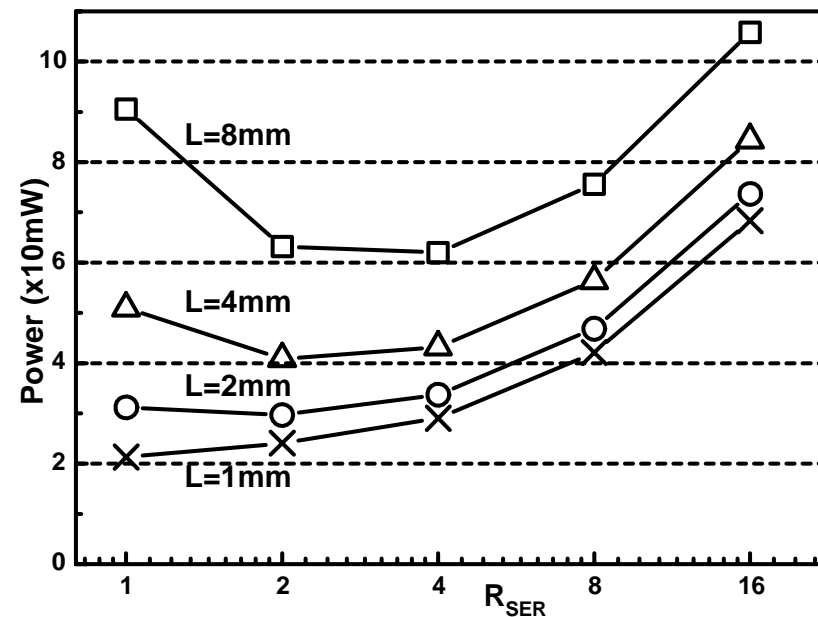
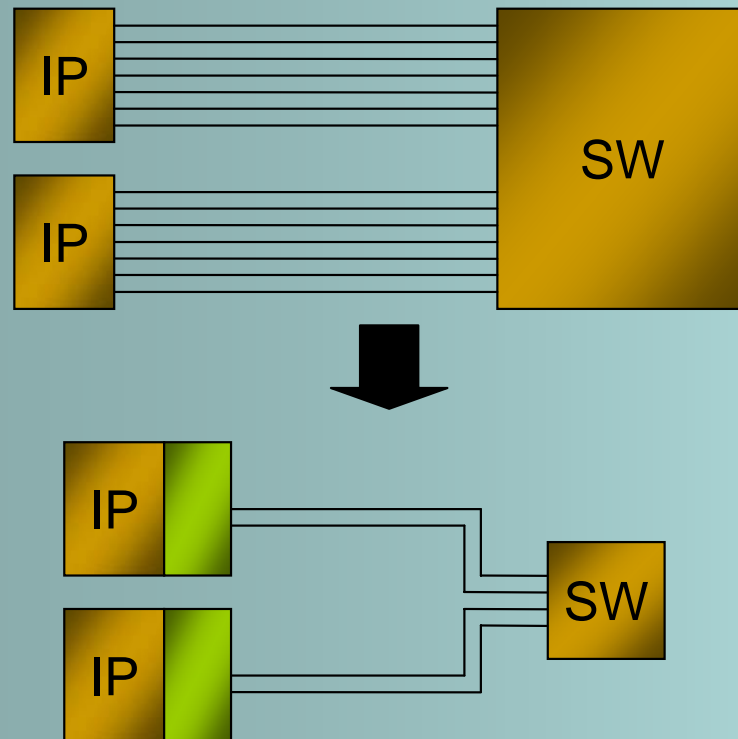
Fully differential TIA



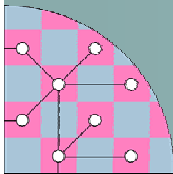
# Interconnection Technology

## ■ On-chip serialization

- Effectiveness of on-chip serialization scheme in terms of power and area cost

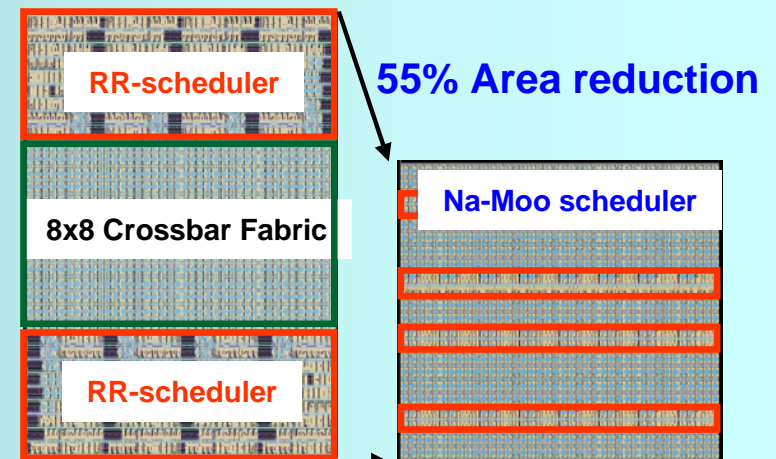
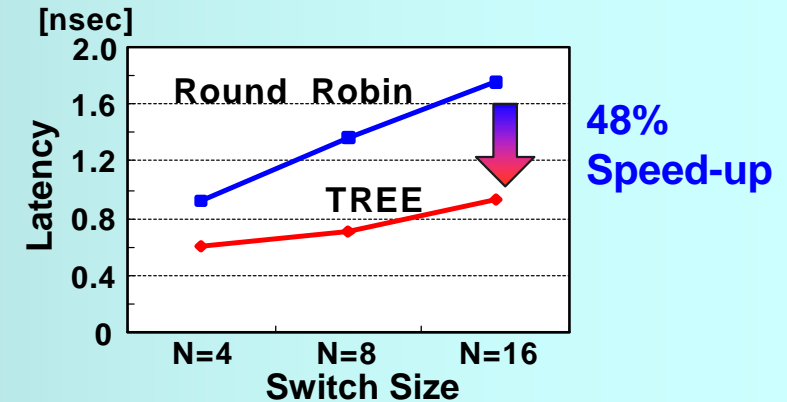
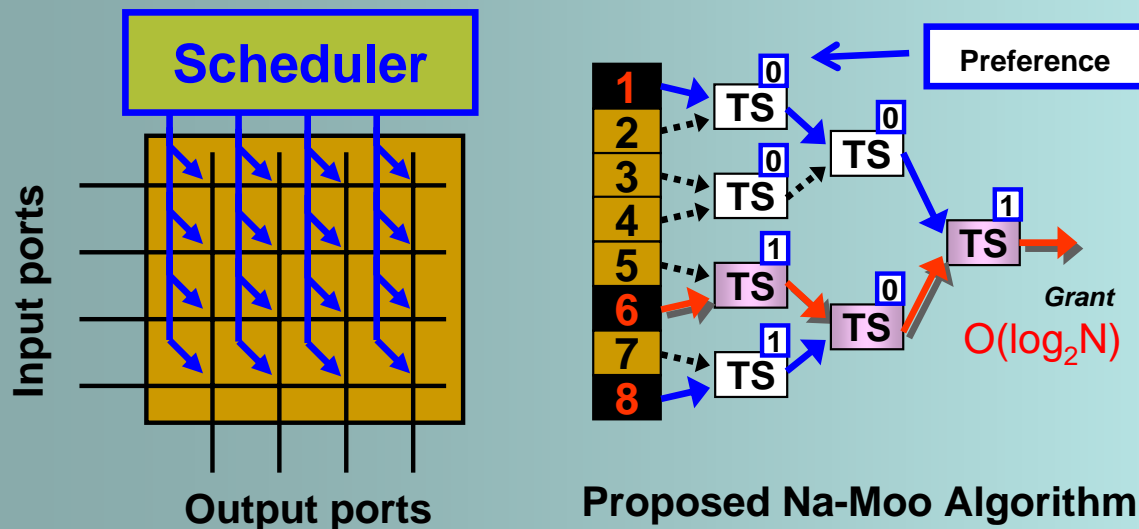


Serialization ratio vs. Power consumption



# Switching Technology

## ■ A Distributed On-chip scheduler



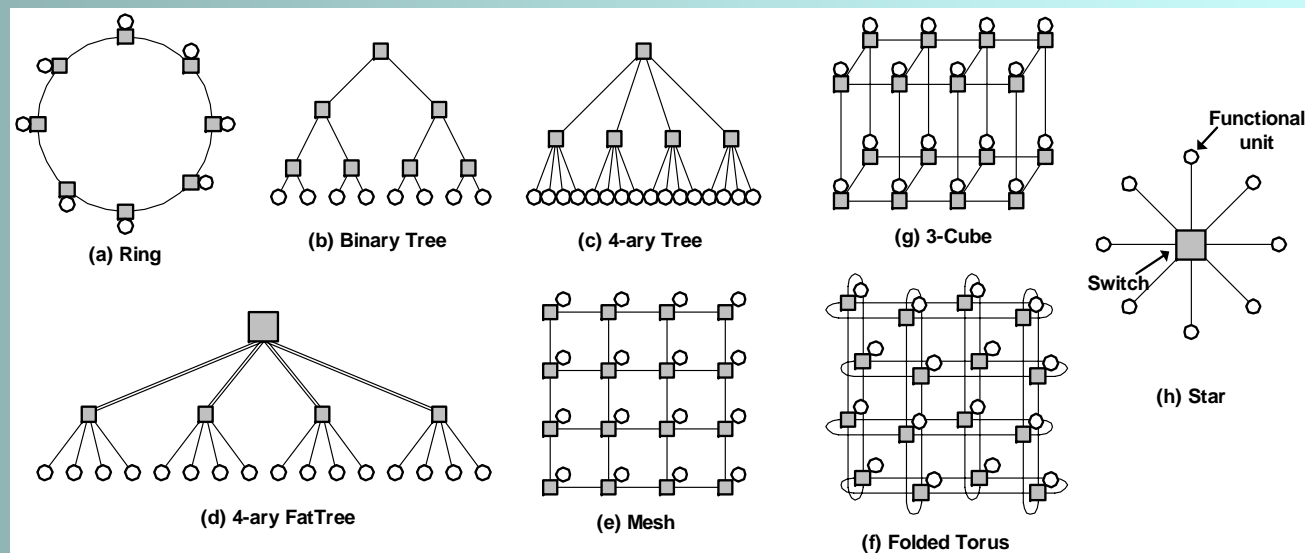
### Related papers

- [1] K. Lee, "A Distributed On-Chip Crossbar Switch Scheduler for On-Chip Network," *CICC 2003*
- [2] K. Lee, "A High-Speed and Lightweight On-Chip Crossbar Switch Scheduler for On-Chip Interconnection Networks," *ESSCIRC 2003*

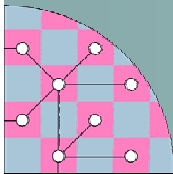
# Networking Technology

## ■ Topology selection

- ❑ Select the optimal one among the sea of topologies
- ❑ Affects the performance and cost of the network
- ❑ Analytic analysis with the consideration of on-chip situation



Possible on-chip network topologies



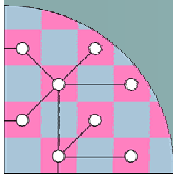
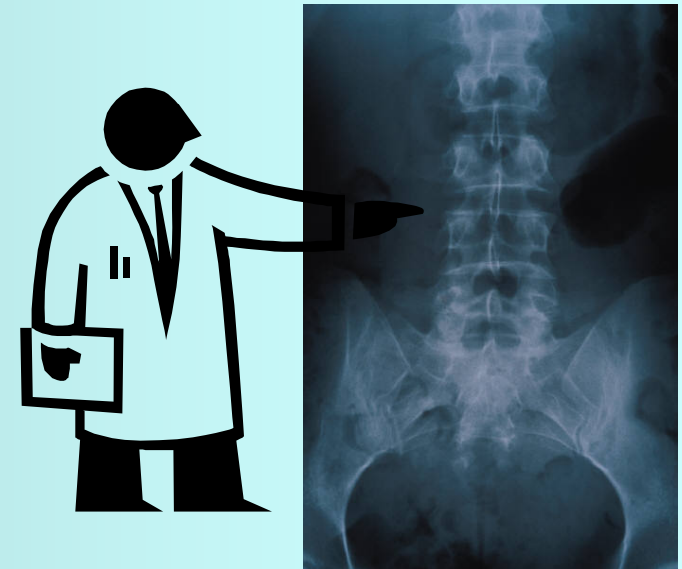


# Project BONE



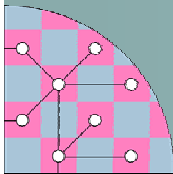
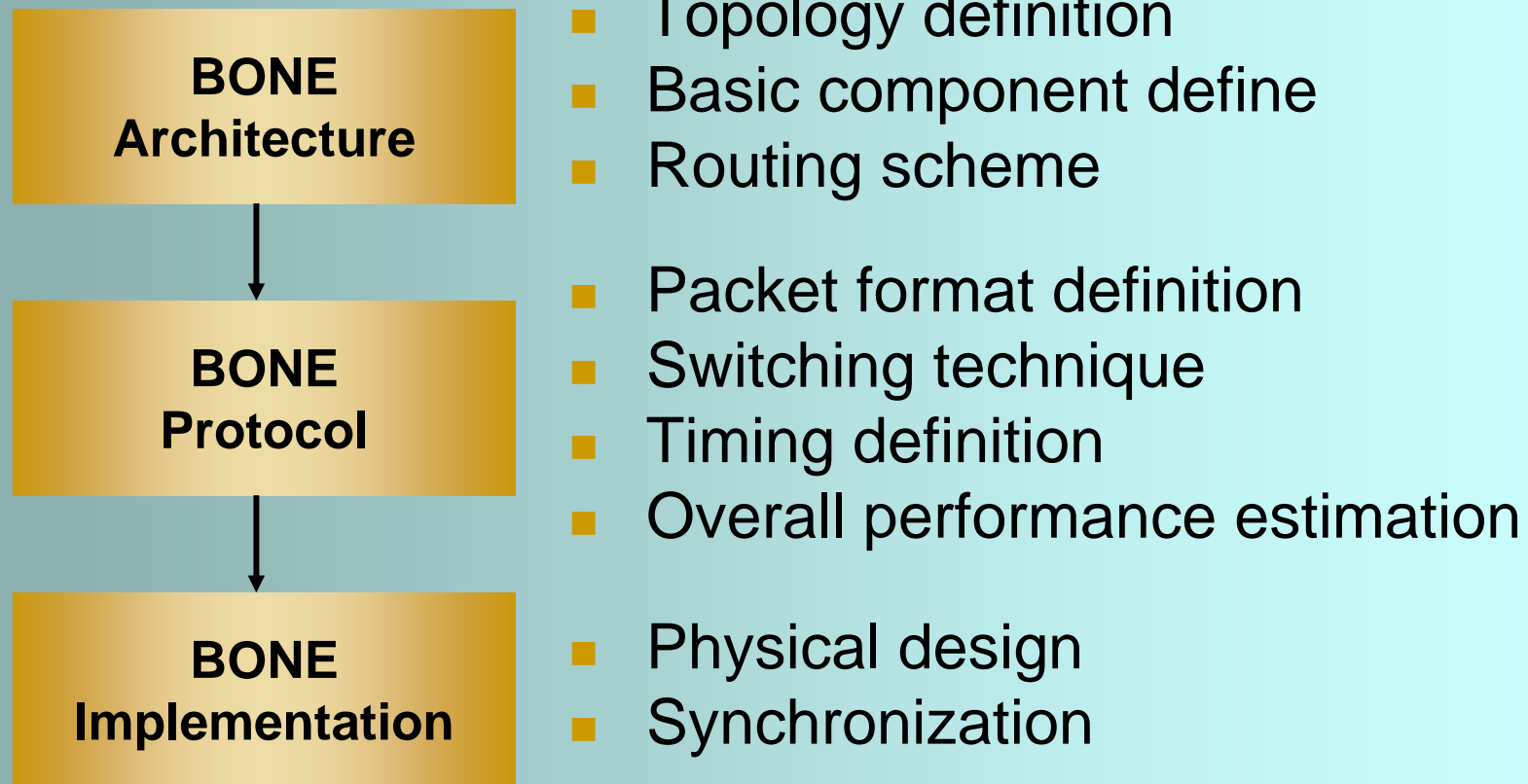
# What is BONE?

- Basic On-chip Network
  - Infrastructure
    - Pre-designed template (Platform)
  - Communication channel
    - Provides high-quality communication channel: scalable bandwidth and controllable latency
  - Interface
    - Heterogeneous IPs interact through the BONE



# BONE-1

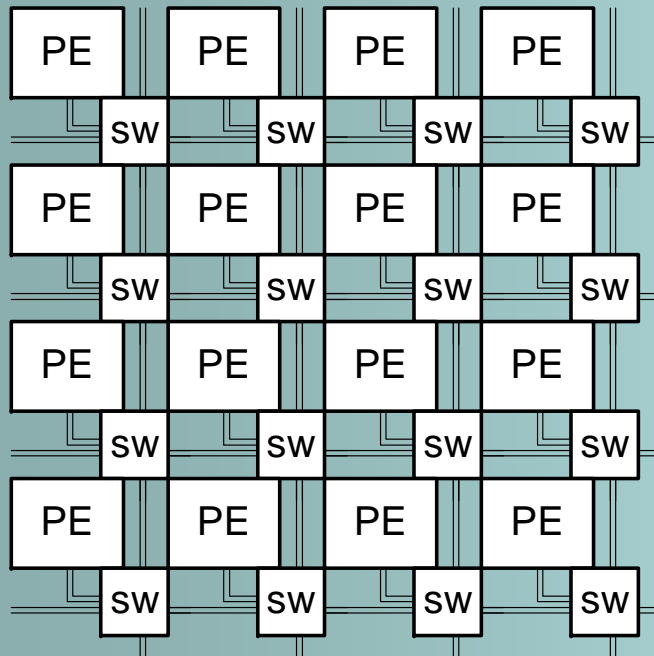
## ■ Development Flow



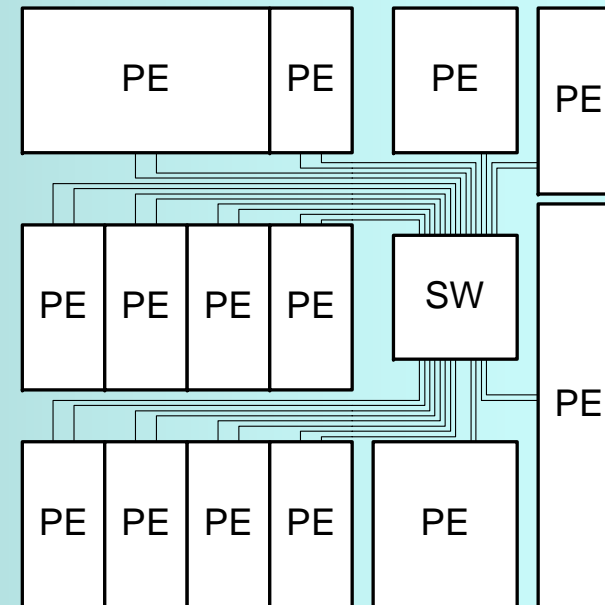


# BONE-1: Architecture

## ■ Star-network with Serialized Links

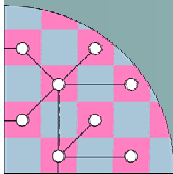


Mesh topology  
in previous works



Star topology of BONE

- Why star topology and serialization ? (Next page...)



# BONE-1: *Architecture* (Cont'd)

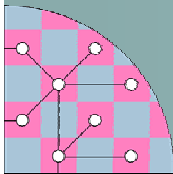
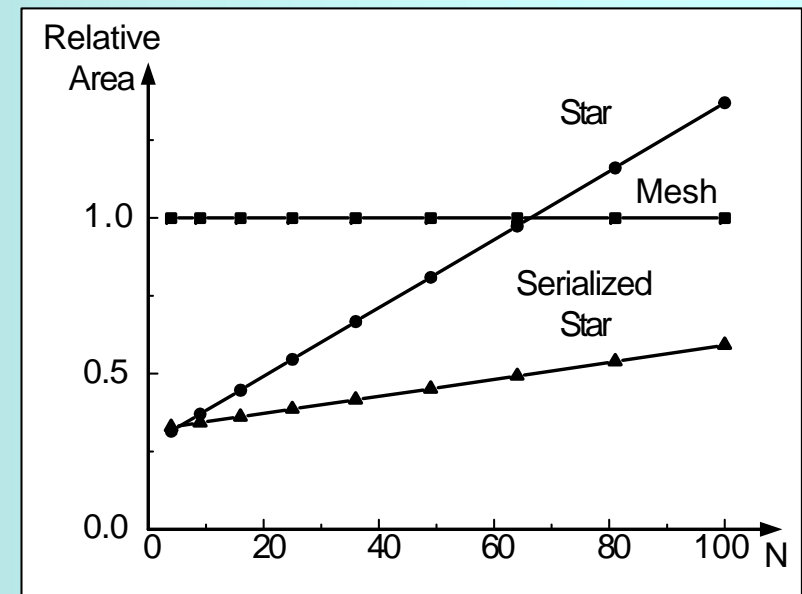
## ■ Advantages

### □ Star-topology

- Supports any layout shape of each processing units
- Routing algorithm is very suitable to on-chip network
- Provides maximum bandwidth and minimum latency

### □ Serialized links

- Area reduction in link wires and switch fabrics
- Power save in switch fabric and link wires



# BONE-1: *Protocol*

## Transport

- Master network interface (MNI)
- Slave network interface (SNI)
- Packet Format

## Network

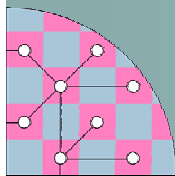
- Source routing scheme
- Route information modification
- Off-chip packet transaction

## Datalink

- Packet serialization
- Flow control

## Physical

- Source synchronous data transaction



# BONE-1: *Protocol* (Cont'd)

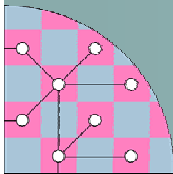
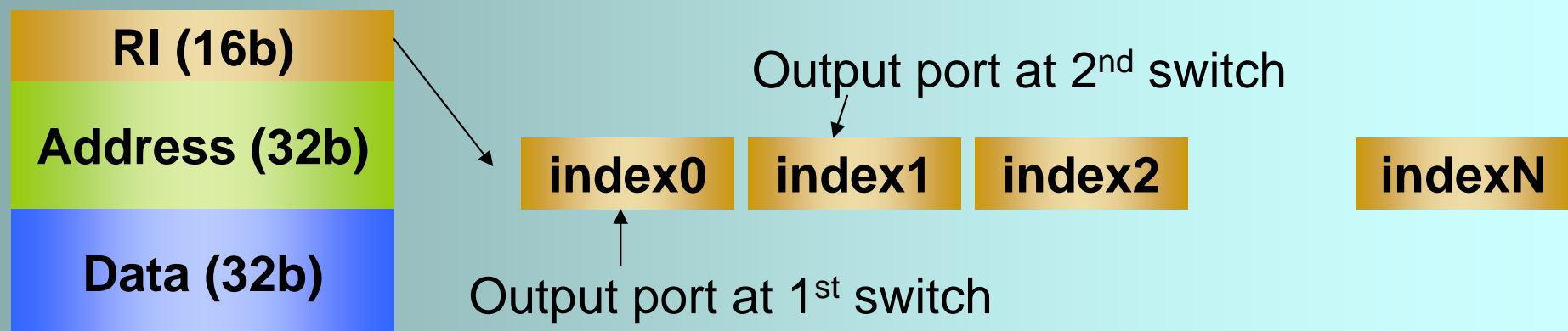
## ■ Packet Format

### □ Fixed length (80-bit)

- Minimize packet processing overhead

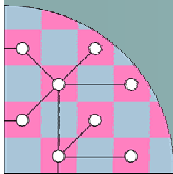
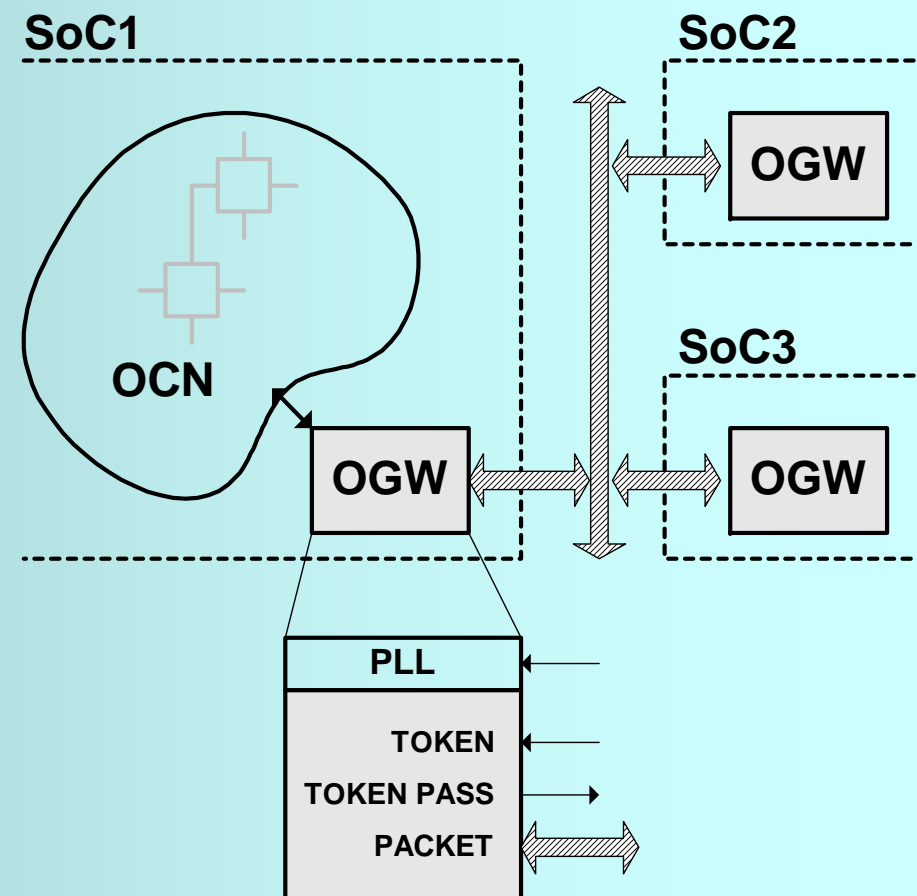
### □ Route Information

- Generated by MNI
- Each index indicates **s** output port at each switch hop

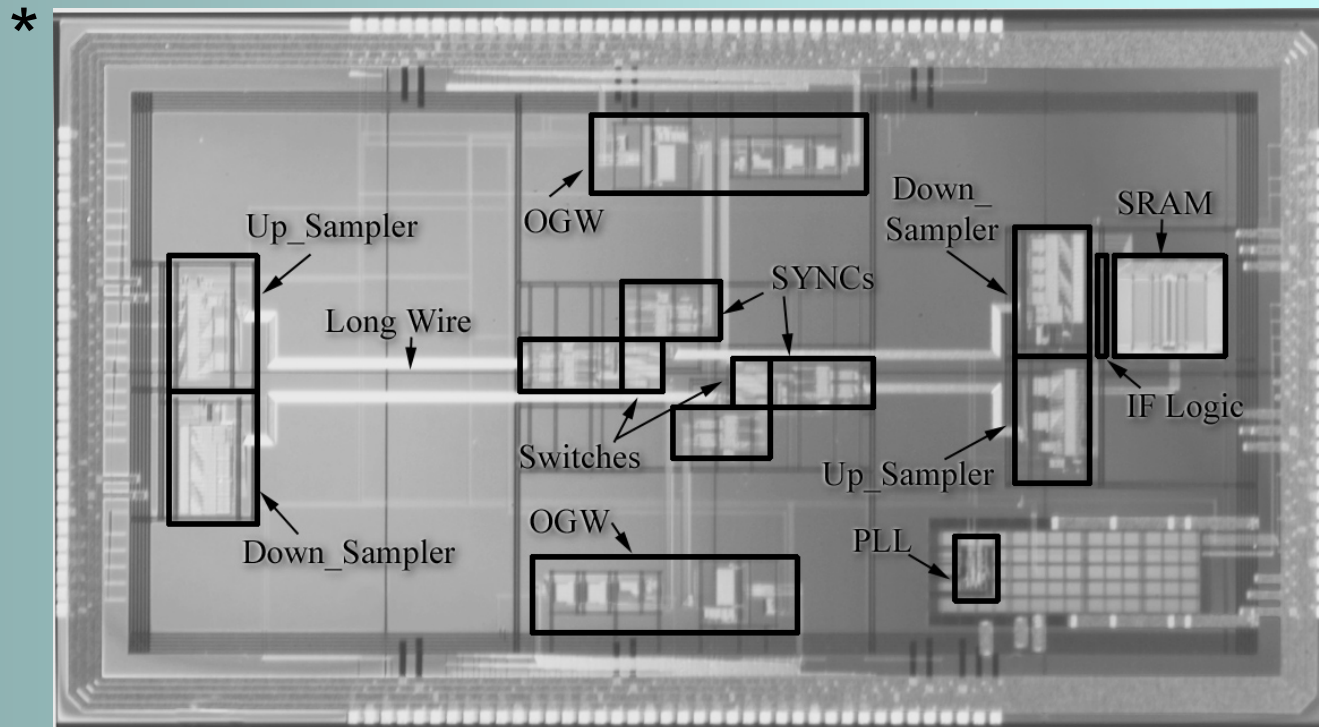


# BONE-1: *Protocol* (Cont'd)

- Off-chip connectivity
  - ❑ Communication between SoCs
  - ❑ BONE defines off-chip gateway (OGW)
- OGW
  - ❑ Synchronized operation using internal PLL
  - ❑ Transaction through off-chip bus
  - ❑ Token-based bus arbitration
  - ❑ Packet routing using RI



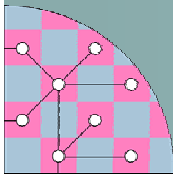
# BONE-1: *Implementation*



- 0.16 $\mu\text{m}$  DRAM technology (Feature size: 0.35 $\mu\text{m}$ )
- 10.8mm x 6mm die size
- 81k transistors + 1kB SRAM
- 264mW at 800MHz, 2.3V

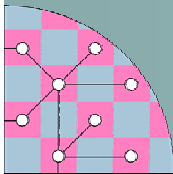
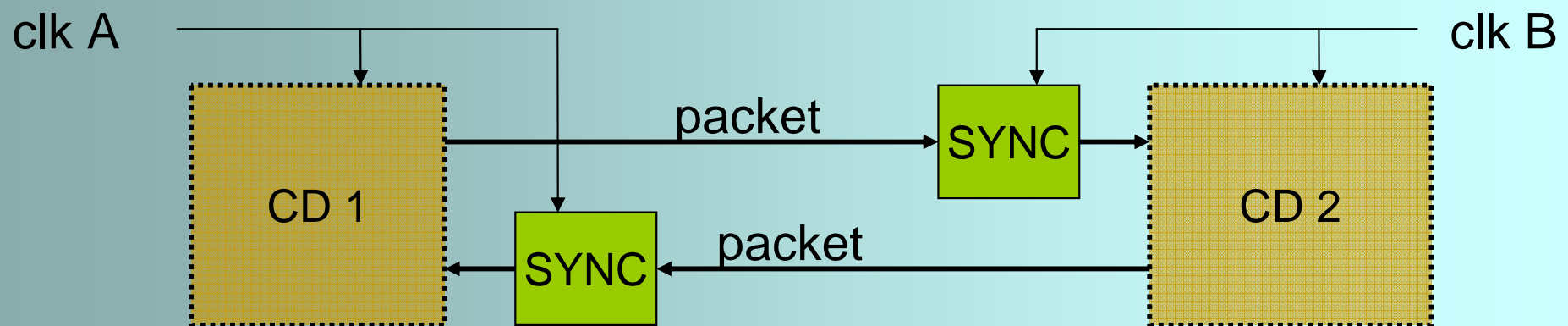


\* Presented in Int. Solid-State Circuit Conference 2003.



# BONE-1: *Implementation* (Cont'd)

- Implementation issue
  - Global synchronization
    - One of the most challenging issues in SoC design
  - BONE-1 supports pleisochronous communication
    - Global synchronization is NOT required
    - Multiple clock domains (CDs) are allowed
    - Signal synchronizers (SYNCs) are inserted among CDs

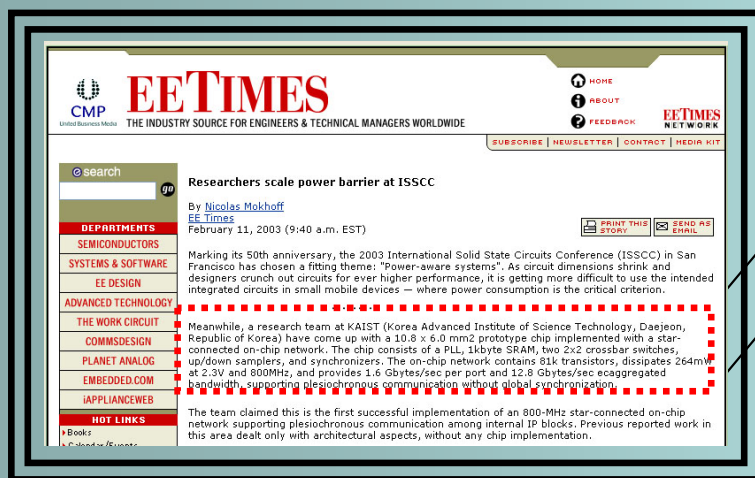




# Press releases



Nikkei Electronics, 2003. 6.  
(On-Chip Network 기술 개발)

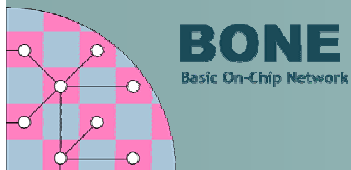


Meanwhile, a research team at KAIST (Korea Advanced Institute of Science and Technology, Republic of Korea) have come up with a 10.8 x 6.0 mm²

EE Times 2003. 2.  
(ISSCC2003)



전자신문  
2003. 6.



**BONE**  
Basic On-Chip Network

*BONE: Flexible System Integration Platform*

# BONE Roadmap

System integration **platform** using OCN

- Aims at easy SoC design
- Operating System

**BONE3**

<2003.3 ~ 2003. 8>

**BONE2**

**Mobile Device SoC** w/ OCN

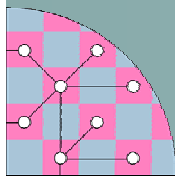
- **IPs: Two RISCs, FPGA, 16kB SRAM..**
- **2-level Star-Topology w/ 1.6GHz links**
- **Plesiochronous Comm.**
- **Low-Power Techniques**
- **BONE-SIM**

<2002. 4 ~ 2002. 6>

**BONE1**

**Prototype** for on-chip networking

- Star-topology with serialized links
- Plesiochronous communication
- Off-chip connectivity

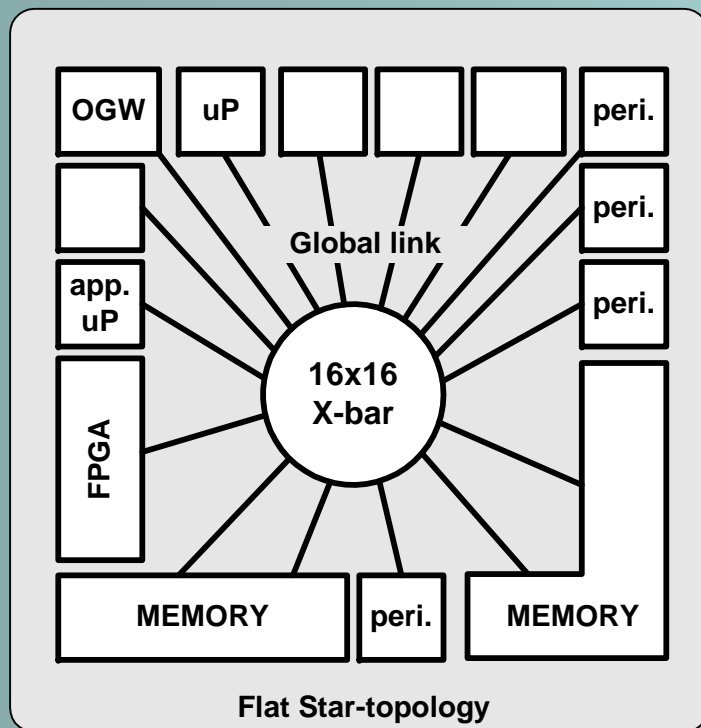


**BONE**  
Basic On-Chip Network

*BONE: Flexible System Integration Platform*

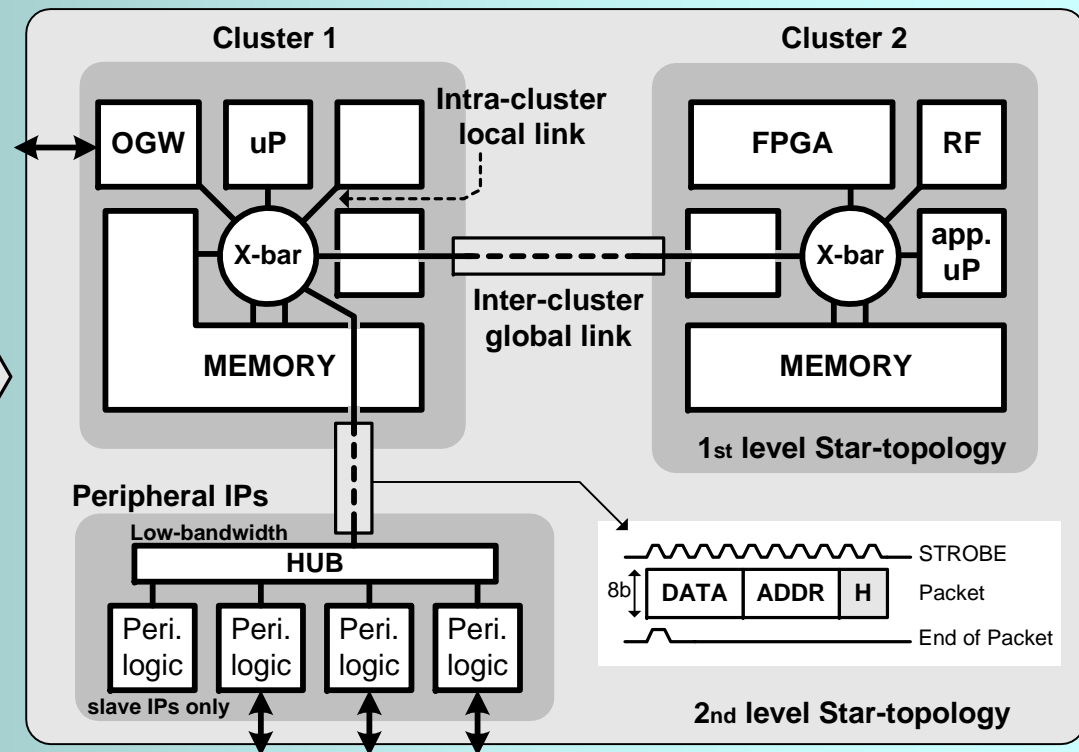
# BONE-2: Architecture *(Confidential!)*

## ■ 2-Level Star-Topology



(a)

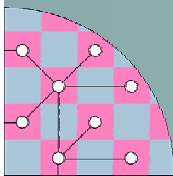
Star-Topology



(b)

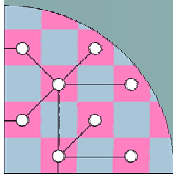
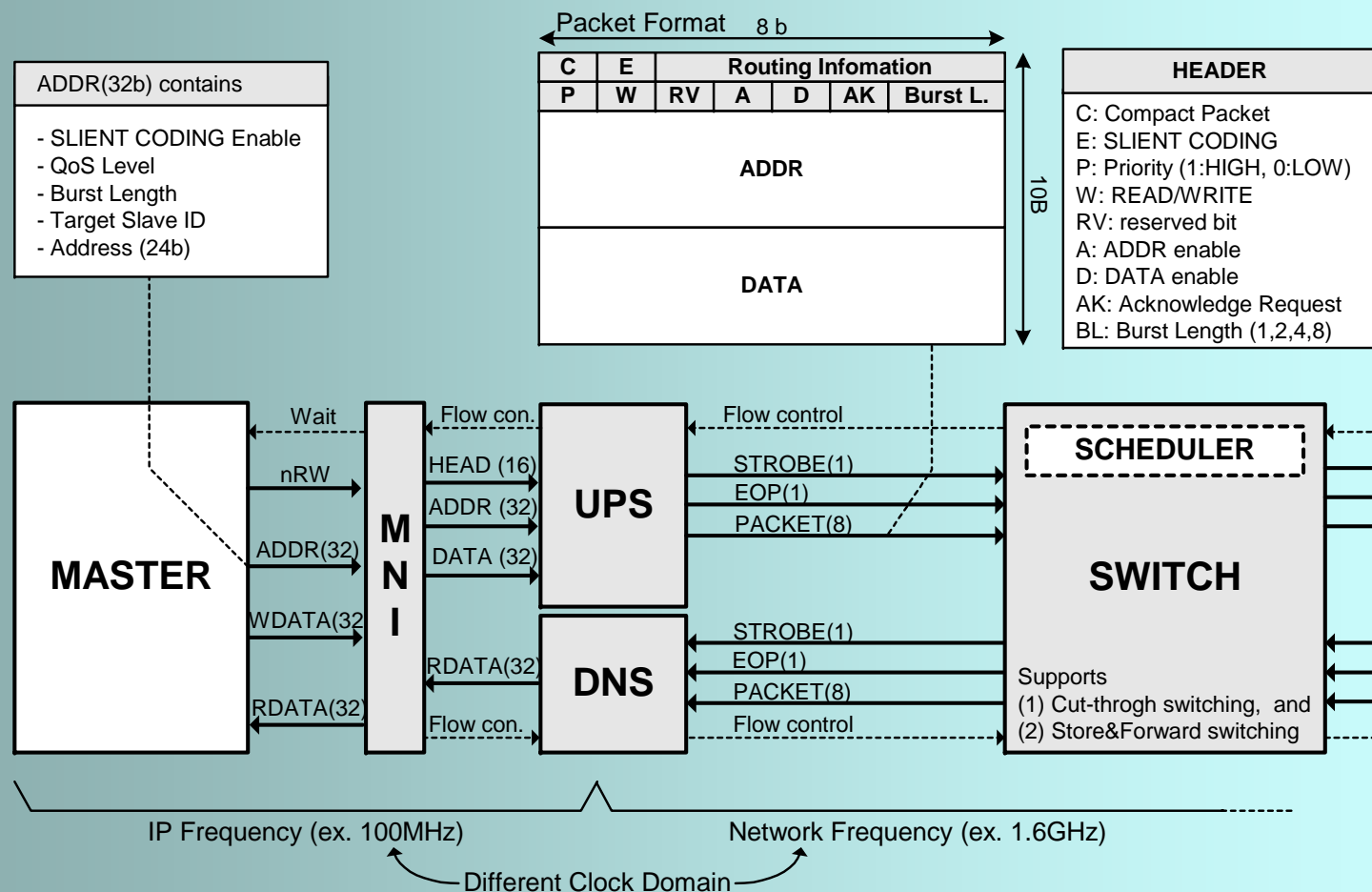
### Cluster-based 2-Level Star-Topology

- : Less global links → Latency & Energy Efficient
- : 47% Power Reduction than (a)



# BONE-2: *Protocol (Confidential!)*

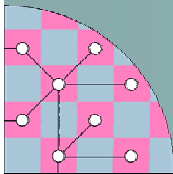
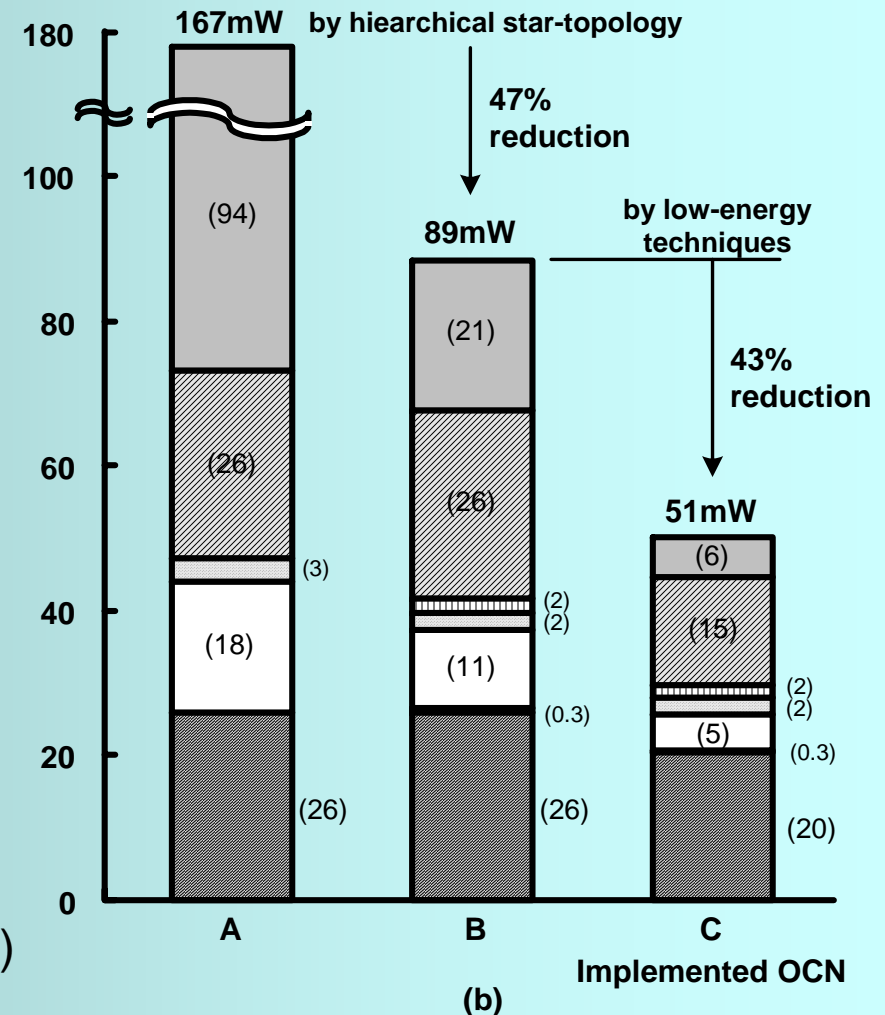
- Burst transactions for large data transfer (BL=1,2,4,8)
- Differentiated Switching (2 level of Quality of Service)
- Flow-control using back-pressure signal
- Acknowledgment packet for reliable communications



# BONE-2: *Low-Power Techniques*

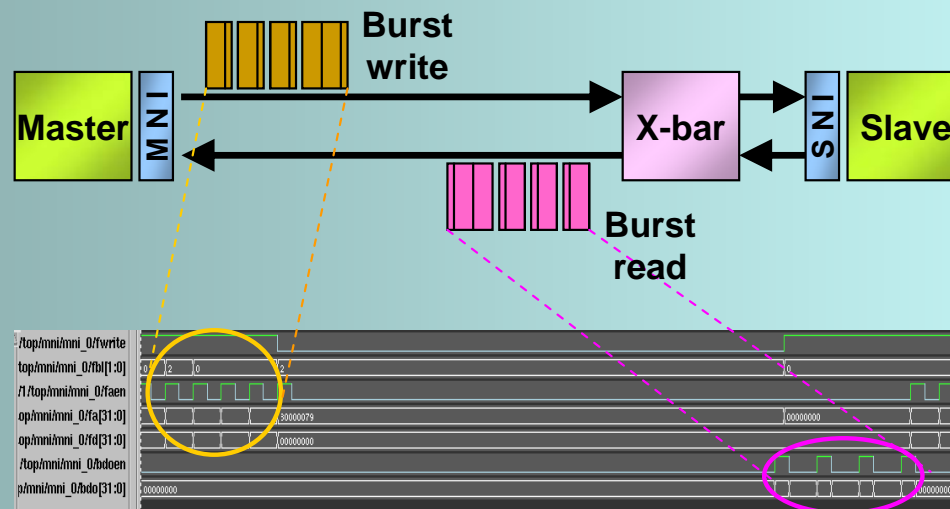
*(Confidential!)*

- 1.6GHz serialized links with  $< 0.6\text{V}$  lower swing.
  - 0.35pJ/bit on 5mm link
  - x3 less power than full-swing,
  - less area w/o repeaters
- Low-Power Switching Fabric  
(*Patent pending..*)
- Serialized Low-Energy Transmission (SLIENT) Coding (*Patent pending*)
- Programmable Power Management
  - Frequency Scaling (1.6GHz  $\rightarrow$  400MHz)

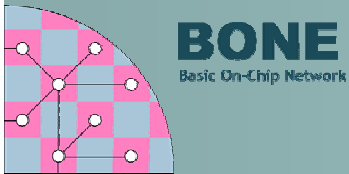


# BONE-2: *BONE-SIM* (Confidential!)

- *BONE-SIM*: BONE-2 Protocol Simulator
  - High-level System Verification
  - Cycle-based Performance Analysis in Plesiochronous Comm.
  - Power & Area Estimation
  - Flexible Configuration
    - Topology (Star, Mesh or arbitrary), Serialization Ratio (1~12)
    - Switching Algorithm, Switch Size, Buffer depth
    - Clock Frequency (Different clk freq. b/w IPs)



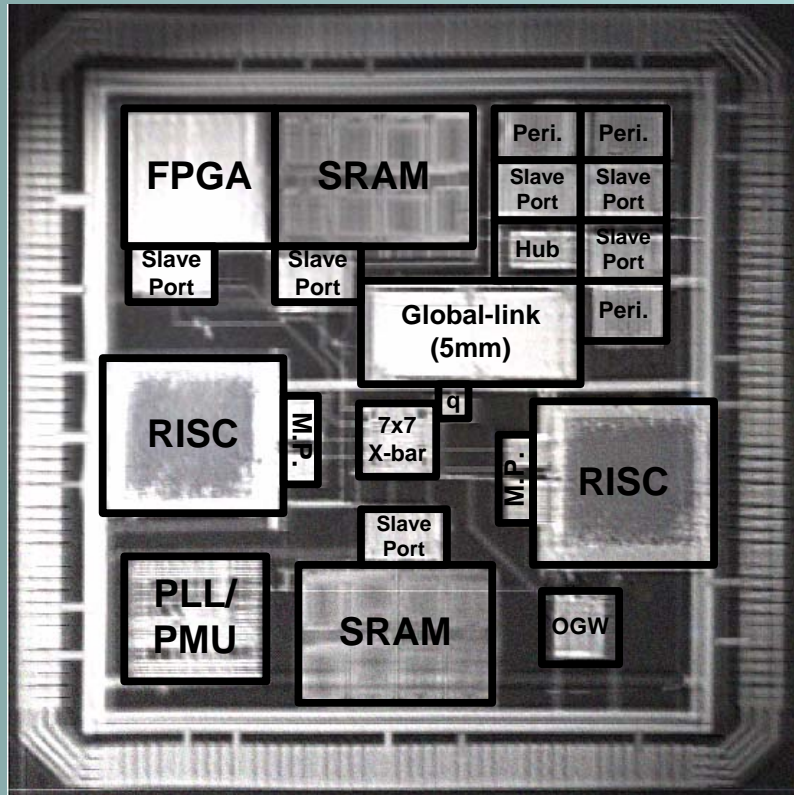
**BONE-SIM**  
Waveform snapshot





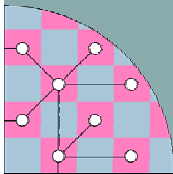
# BONE-2: *Implementation* (Confidential!)

\*



- 0.18 $\mu$ m CMOS technology
- 5mm x 5mm
- Integrated IPs:
  - Two RISCs,
  - Two 8kB SRAMs,
  - On-chip FPGA,
  - Peripheral Logic,
  - Off-chip Gateway
- 50mW @ 1.6GHz, 1.6V/0.6V
  - w/ various low-power techniques

\* Accepted for Presentation in **ISSCC 2004**.

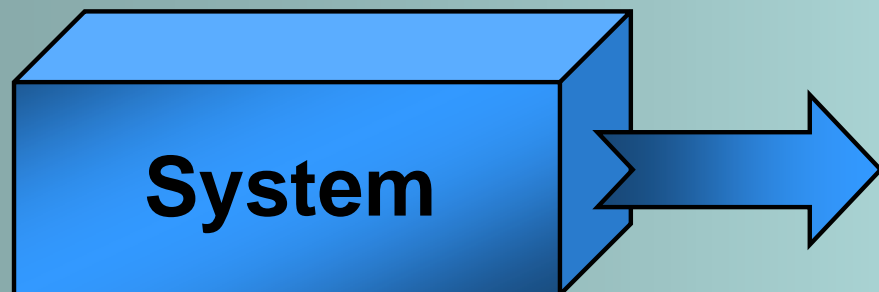




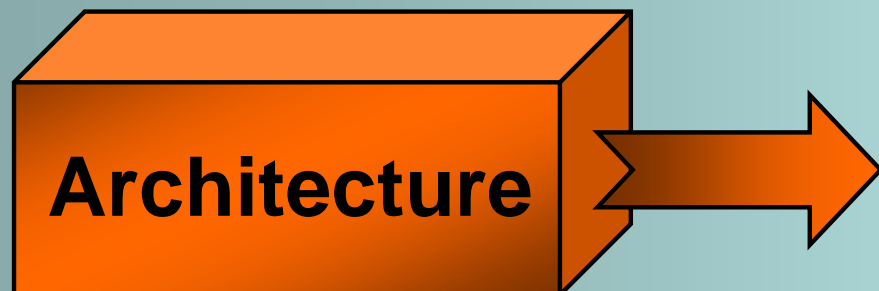
The background of the slide is a repeating pattern of light blue circuit board layouts. Each layout shows a complex arrangement of components, including integrated circuits, resistors, and capacitors, connected by a network of fine lines representing traces. The pattern is uniform and covers the entire slide area.

# Recent Research Topics

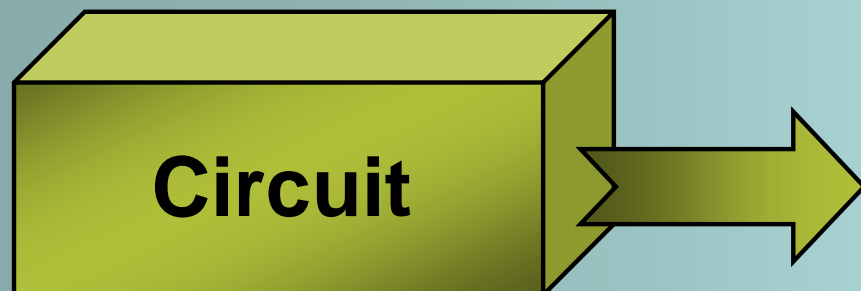
# Recent Research Topics



- Applications
- Operating System S/W
- OCN-based SoC Platform
- Plug & Play
- SoC Design Methodology (SoC WIZARD™)



- Topology
- OCN-Protocol
  - ❖ BONE-SIM
  - ❖ BONE-Emulator



- Low-Power Implementation
- Plesiochronous Communications
- On-Chip Serialization

